

CUSTOMER NO.: 24498
Ser. No. 09/936,479

PATENT RECEIVED
PD990014 CENTRAL FAX CENTER
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Remarks/Arguments

Claims 1-9 are pending. Claims 1-9 stand rejected.

Claims 1 and 5 have been amended to more clearly and distinctly claim the subject matter that applicants regard as their invention. No new matter is believed to be added by the present amendment.

Rejection of claims 1-8 under 35 USC 103(a) as being unpatentable over Boyer et al. (US Pat. No. 5410546) (hereinafter Boyer) in view of Hamada (JP 411,004,255A).

The MPEP 2143 requires that to establish a *prima facie* case of obviousness, the prior art references when combined must teach or suggest each and every claim limitation.

Applicants submit that for at least the reasons discussed below, the combination of Boyer and Hamada fail to disclose each and every limitation of amended claims 1-8, and as such, these claims are not rendered obvious by Boyer and Hamada.

On page 3 of the current Office Action, it is argued that col. 13, lines 1-23 of Boyer describes applicants' claimed:

"carrying out a modulo-n counting of the data blocks in order to determine the data source packet boundaries" as recited in claims 1 and 5.

However, a review of the cited sections of Boyer teaches that the counter 415, Fig. 4, is a byte counter that is used internally to determine when a page buffer of a given fixed size has been filled up. The counter is loaded with the value of the page size, prior to each countdown. This counter is not a modulo-n counter and does not provide any determination of data source packet boundaries. Rather, it is used to determine the fill status of a page buffer. In contrast, applicants' claims 1 and 5 recites modulo-n counting of the data blocks in order to determine the data source packet boundaries.

The invention in Boyer, as described in col. 13, provides a counter 415 which determines when a page buffer in the DRAM ARRAY 410 has been filled. The counter is loaded internally by the State Control Logic 411 with a value from a page size register 412 at the start of filling a page buffer. The counter 415 is decremented to zero indicating when a page buffer is completely filled.

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There is no description of the features as claimed by applicants, for example, a modulo-n counting of data blocks, because Boyer describes loading the counter with a count value at the end of each countdown.

Also Boyer is silent with regard to counting of the data blocks in order to determine the data source packet boundaries, because in Boyer there is no data blocks forming a source packet of fixed length. If one compares the page buffers to the data blocks, these page buffers do not have any particular relationship to the data included in the bus packet. Boyer does not mention a defined number of page buffers forming a source packet of a fixed length, and carrying out a modulo-n counting of the data block to determine the source packet boundaries.

Furthermore, the Office Action points to col. 13, lines 30-64 and col. 16, line 66 through col. 17, line 6 of Boyer to describe applicants' claimed feature:

"the beginning of a new data source packet is signaled to a memory management device at the beginning of the next counting interval."

However, as described in cols. 13, 16 and 17 of Boyer the State Control Logic prepares for a new packet when it senses the End Of Header (EOH) signal. Boyer does not describe the counter indicating the beginning of a new data source packet, Boyer determines the new packet by sensing the EOH. Boyer only suggests that when Counter 215 is decremented to zero an end of page arises and the State Control Logic 214 reloads the page size into the Counter 215.

The above claimed features are also lacking in Hamada because the counter in Hamada likewise does not carry out a modulo-n counting of the data blocks in order to determine the data source packet boundaries.

The counter in Hamada counts the number of 4-byte data words from the variable length source packet. Hamada describes a header generation section 104 is connected to the down counter 103. The value of the down counter 103 is used by the header generation section 104 to produce the fixed length frame header for the fixed length frame outputted from the output selector 105.

In contrast, applicants' claims 1 and 5 recite a modulo-n counting of the data blocks in order to determine the data source packet boundaries. The counter in Hamada does not determine a packet boundary of the data source packet.

In addition, the down counter 103 disclosed in the Hamada counts "read-out units" identified to be quadlet words (4-byte data words).

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In contrast applicants' claimed invention recites data block counting which is different from the counter disclosed in Hamada. As recited in applicants' claimed invention a data block consists of a plurality read-out data units, the plurality being a fixed amount. The counting of the defined data block in applicants' claimed invention is clearly different from Hamada's counting of read-out units of 4-byte data words.

From the foregoing, one skilled in the art would not find applicants' claimed invention obvious from the teaching of Boyer and Hamada, since the combination of references fail to teach or suggest all the claimed features.

Claim 5 recites similar features found in claim 1 in apparatus form. For at least the foregoing reasons, applicants submit that the combination of Boyer and Hamada fail to disclose or suggest each and every limitation of claims 1 and 5 as required to render a claim obvious; therefore, it is respectfully requested the rejection be withdrawn.

Claims 2-4 depend from claim 1 and claims 6-8 depend from claim 5. Each dependent claim includes at least the above distinguishing features of the respective independent claim. Each dependent claim also includes additional distinguishing features. For at least the forgoing reasons it is respectfully requested the rejection of the dependent claims likewise be withdrawn.

Rejection of claim 9 under 35 USC 103(a) as being unpatentable over Boyer, Hamada in view of Lo et al. (previously cited, hereinafter Lo)

Lo is cited as teaching the use of a data bus designed according to IEEE 1394, and the Office Action alleges that it would be obvious to combine the teachings of Boyer, Hamada and Lo. However, applicants submit that even assuming arguendo that Boyer, Hamada and Lo are combined in the manner suggested, the suggested combination still fails to cure the defects of Boyer and Hamada as applied to present claim 5, and thus, present claim 9 remains patentably distinguishable over the combination of Boyer, Hamada and Lo.

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Having fully addressed the Examiner's rejections, Applicants submit that the present application is in condition for allowance and respectfully request such action. If a fee is due, please charge the fee to Deposit Account 07-0832. Should any questions arise regarding any of the above, the Examiner is requested to contact the undersigned at 609-734-6815.

Respectfully submitted,

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